Phase-Locked Loop

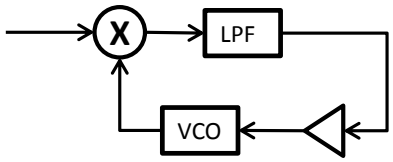
Modules: VCO (2), Multiplier, Quadrature Utilities, Wideband True RMS Meter, Tuneable LPF, Digital Utilities, Noise Generator, Speech, Headphones

0 Pre-Laboratory Reading

Phase-locked loops have many uses in electronic instrumentation. They are used for synchronizing one oscillator with another (for example, carrier synchronization in a receiver). Phase-locked loops are employed in frequency synthesizers. A carrier with FM can be demodulated with a phase-locked loop.

0.1 Synchronization with a Phase-Locked Loop

The simplest type of phase-locked loop is a feedback circuit that looks like this:



The input signal is a sinusoid (or at least contains a sinusoid, perhaps with other signal components). The VCO produces a sinusoid. When the loop is tracking properly, these two sinusoids have the same frequency. The multiplier produces a difference-frequency term and a sum-frequency term, but only the former passes through the lowpass filter. The output of the filter is an error signal, and it is amplified and then placed at the input to the VCO, completing the loop.

The VCO used in this experiment has a negative sensitivity. A positive voltage on the input causes the output frequency to have less than its nominal value (its value with zero input), and a negative voltage on the input results in an output frequency that is larger than the nominal value. A Buffer Amplifier with negative gain is used to amplify the error signal before it is placed on the VCO input. Therefore, a positive error signal (at the filter output) causes the VCO output frequency to be larger than its nominal value.

A little trigonometry shows how this loop works. Here the input sinusoid (carrier) is modeled as

$$\text{carrier} = \sin(2\pi f_c t + \theta_c) \tag{1}$$

and the VCO output is modeled as

$$\text{VCO output} = 2\cos(2\pi f_c t + \theta_v) \tag{2}$$

The phase θ_c of the carrier and the phase θ_v are implicit functions of time. It should be noted that Eq. (1) models the carrier with a sine function and Eq. (2) models the VCO output with a cosine function. Therefore, even if $\theta_v = \theta_c$, the carrier and the VCO output are not in phase; instead the VCO output leads the carrier by 90° (when $\theta_v = \theta_c$).

For this simple phase-locked loop, the error signal is the difference-frequency term produced by the multiplier. This is:

$$\text{error signal} = \sin(\theta_c - \theta_v) \tag{3}$$

Experience shows that this error signal will be small when the loop is properly tracking. It is assumed here that $\theta_v \cong \theta_c$. The sine of a small angle is approximately the angle (in units of radians).

$$\text{error signal} \cong \theta_c - \theta_v \tag{4}$$

Three possibilities are now examined, as outlined in Table 1. If $\theta_v = \theta_c$, the error signal is zero and the VCO will not try to move away from this operating point. If $\theta_v < \theta_c$, the error signal is positive and the VCO will respond by increasing the rate at which it produces phase (the VCO frequency will increase). In other words, if θ_v has fallen behind θ_c, a positive error signal will be generated, which will prod the VCO to catch up. If $\theta_v > \theta_c$, the error signal is negative and the VCO will respond by decreasing the rate at which it produces phase. In other words, if θ_v is already ahead of θ_c, a negative error signal will be generated, which will prod the VCO to slow down. In summary, the feedback action of the loop will tend to drive the error signal toward zero, as long as the error signal is already small (that is, when the loop is properly tracking).

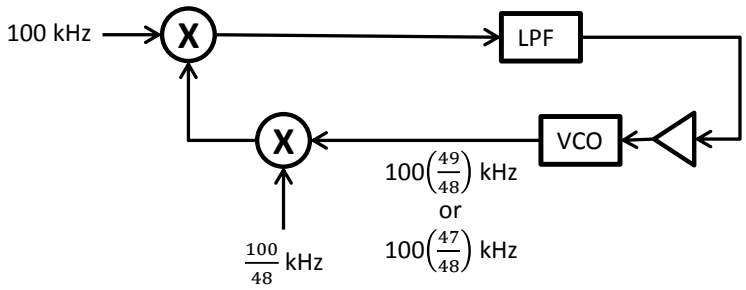
Table 1: Response of VCO to error signal

condition	error signal	response
$\theta_v = \theta_c$	0	no change
$\theta_v < \theta_c$	positive	increase θ_v
$\theta_v > \theta_c$	negative	decrease θ_v

For this simple phase-locked loop, it is important that the nominal frequency of the VCO match closely the carrier frequency. If this is not the case, θ_v will not track θ_c. When θ_v is tracking θ_c, as described above, the loop is said to be in *phase lock*. When this loop is in phase lock, the VCO frequency will match the carrier frequency and the VCO will lead the carrier by 90°, as indicated in Eqs. (1) and (2). The VCO is then said to be *synchronized* to the carrier.

0.2 Frequency Synthesis of Analog Sinusoid

A more complicated phase-locked loop can be used for frequency synthesis. Here is an example:



The feedback action of this loop will drive the VCO such that the difference frequency produced by the upper multiplier is zero. In other words, the loop (when in phase lock) will ensure that the two inputs to this multiplier have the same frequency.

What will be the VCO output frequency? One possibility is that the VCO frequency *minus* $(100/48)$ kHz will equal 100 kHz. The other possibility is that the VCO frequency *plus* $(100/48)$ kHz will equal 100 kHz. These are the two possible lock points.

$$\text{VCO frequency} = 100 \text{ kHz} + (100/48) \text{ kHz} = 100(49/48) \text{ kHz} \cong 102.083 \text{ kHz}$$

or

$$\text{VCO frequency} = 100 \text{ kHz} - (100/48) \text{ kHz} = 100(47/48) \text{ kHz} \cong 97.917 \text{ kHz}$$

In the experiment, the 100-kHz and the $(100/48)$-kHz sinusoids are both derived within the Master Signals module from a crystal oscillator. Both are stable frequencies. The loop will cause the VCO to produce one of the frequencies listed above, and the stability of the frequency produced by the VCO will reflect the superior stability of the crystal oscillator and not the inferior stability that is inherent to the VCO (which has no crystal). Hence, a new, stable frequency has been synthesized.

If you want this frequency synthesizer to produce $100(49/48)$ kHz, you will tune the nominal frequency of the VCO to approximately 102.083 kHz. If you want instead $100(47/48)$ kHz, you will tune the nominal frequency of the VCO to approximately 97.917 kHz.

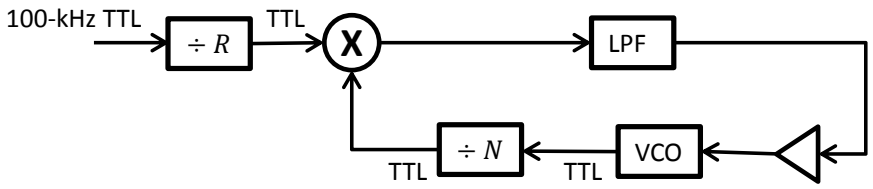
0.3 Frequency Synthesis of Data Clock

A clock circuit that uses a crystal can generate a stable frequency. The 100-kHz TTL signal that is available on the Master Signals panel is an example of this kind of stable clock. Such clocks are useful for providing timing.

There is a need to generate new clock frequencies from a stable clock. The frequency dividers on the Digital Utilities module can generate new clock frequencies by dividing the input clock frequency by a whole number: 2, 3, or 4.

A phase-locked loop can be used with two frequency dividers to generate a clock frequency that is a positive, rational number times the reference frequency. (A positive, rational number is one whole number divided by another.) In this case, the reference frequency is that of the 100-kHz TTL clock.

A circuit that generates a new TTL clock having frequency $(N/R) \times 100$ kHz from a reference clock of frequency 100 kHz is shown below:



Here is the basic idea of how this circuit works. The TTL clock at the output of the $\div R$ device has a frequency of $100/R$ kHz. When the phase-locked loop is in phase lock, the two inputs to the multiplier will have the same frequency. The feedback action of the loop ensures this (when the loop is properly tracking). Therefore, the output of the $\div N$ device has, under these circumstances, a frequency of $100/R$ kHz and the input of the $\div N$ device, which is also the output of the VCO, has a frequency of $(N/R) \times 100$ kHz.

0.4 FM Demodulation with Phase-Locked Loop

A phase-locked loop can be used to demodulate a carrier with FM. When the carrier is applied to the input of the loop, the feedback action of the loop causes the VCO frequency to match that of the carrier, including the frequency deviation caused by the message. The VCO is a frequency modulator; it can generate the correct frequency, including the frequency deviation caused by the message, only if the loop error signal is a scaled replica of the original message.

1 Phase-Locked Loop

Make sure the switch on the VCO module's PCB is set to "VCO". Set the toggle switch on the front panel of the VCO module to "HI". Place the VCO output on the input of the Frequency Counter. With the gain knob on the VCO module set in the fully counterclockwise (zero-gain) position, use the frequency knob to set the VCO output frequency to approximately 100 kHz. Observe the VCO output frequency for a few minutes. It should be clear that the VCO does not have good frequency stability.

Connect the Variable DC output to the VCO input. Adjust the DC source to $+1$ V with the help of the RMS Meter. (Check the Variable DC output on the oscilloscope, to make sure that it is $+1$ V, rather than -1 V.) Rotate the gain knob on the VCO clockwise until the VCO output frequency decreases by 1 kHz from its nominal frequency. The sensitivity is now set for -1 kHz/V. You should keep the VCO sensitivity at -1 kHz/V for the remainder of this experiment. Disconnect the Variable DC source from the VCO.

You will use a Tuneable LPF module for the loop filter. Adjust the bandwidth of this filter to approximately 10 kHz. (The Tuneable LPF's clock output has a frequency equal to 100 times the bandwidth.) Use the Noise Generator module to get a quick display of $|H(f)|$.


Channel A: Tuneable LPF output, showing $|H(f)|$

Build a simple phase-locked loop. The carrier and the VCO output will be multiplied together, and this product will pass through the loop filter. The filter output should be connected to a Buffer Amplifier, and the amplifier output should be connected to the VCO input. This completes the loop. Because the Buffer Amplifier has negative gain and the VCO has a negative sensitivity, a positive error signal (at the filter output) will cause an increase in the VCO output frequency.

Place a 100-kHz sinusoid (Master Signals) on the input of the phase-locked loop. Place a copy of this carrier on Channel A. Place a copy of the VCO output on Channel B. Use the carrier as the trigger source. Monitor the VCO output frequency on the Frequency Counter.

In order for this loop to achieve phase lock, the gain in the loop must not be too small or too large. There is a happy medium that results in phase lock. You can use both the gain of the Buffer Amplifier and the gain of the Tuneable LPF to adjust the gain in the loop. Adjust the loop gain until the loop achieves phase lock.

You can recognize phase lock as follows. The Frequency Counter will indicate that the VCO output frequency is a stable 100 kHz, matching that of the carrier. The oscilloscope will have a stable display for the VCO output (as well as for the 100-kHz carrier). The stable oscilloscope display is the more reliable indicator of phase lock.

If you have any difficulty obtaining phase lock using only adjustments in the loop gain, make slight changes to the VCO nominal frequency (with the loop closed) using the tuning knob on the VCO.


Channel A: 100-kHz carrier (input to phase-locked loop)
Channel B: VCO output

Measure the phase difference between the VCO output and the carrier. You should find that the VCO output leads the carrier by approximately 90°.

Switch the oscilloscope to XY View. The axes of the displayed ellipse should be approximately horizontal and vertical. This is another indication that there is a 90° phase difference between these two sinusoids. (However, you must view the signals as a function of time to determine which sinusoid leads.)

- Channel A: 100-kHz carrier (input to phase-locked loop)
  Channel B: VCO output

2 Frequency Synthesis of Analog Sinusoid

Build a frequency synthesizer that can generate either a $100(49/48)$ kHz or $100(47/48)$ kHz analog sinusoid. The switch on the VCO module's PCB should be set to "VCO", and the toggle switch on the front panel should be set to "HI". The VCO should have a sensitivity that is adjusted to -1 kHz/V. (This can be accomplished as described earlier, applying $+1$ V to the VCO input and adjusting the gain knob on the VCO for a 1-kHz reduction in the VCO output frequency.) Use a Tuneable LPF with its bandwidth adjusted to 10 kHz for the loop filter. Use a Buffer Amplifier between the filter and the VCO input. This frequency-synthesizer loop requires two multipliers; at least one of these must be on a Quadrature Utilities module. This frequency synthesizer requires two inputs: A 100-kHz sinusoid and a $(100/48)$-kHz sinusoid, both on the Master Signals panel. (The second of these is labeled as 2 kHz, but it is actually generated within the Master Signals panel by dividing the frequency of a 100-kHz sinusoid by 48.)

Place a copy of the 100-kHz sinusoid (Master Signals) on Channel A. Place a copy of the VCO output on Channel B. Use a $(100/48)$-kHz TTL signal as an external trigger source. The following paragraph discusses the availability of a $(100/48)$-kHz TTL signal.

There are two versions of the TIMS-301C instrument: an older version and a newer one. In the newer version, a $(100/48)$-kHz TTL signal, called 2 kHz TTL, is available on the Master Signals panel. In the older version, a $(100/48)$-kHz TTL signal is not available. With this older instrument, you can generate a $(100/48)$-kHz TTL signal from the $(100/12)$-kHz TTL signal, called 8.3 kHz TTL, using a divide-by-4 on the Digital Utilities module.

With a $(100/48)$-kHz TTL trigger signal, every sinusoid having a frequency that is an integer multiple of $(100/48)$-kHz can be made stable in the oscilloscope display. The 100-kHz sinusoid will therefore be stable if proper triggering is done. When the loop is locked, the VCO output will also be stable, whether the frequency is $100(49/48)$ kHz or $100(47/48)$ kHz. When using a TTL signal as the trigger source, it is necessary that the trigger level be set to a value greater than 0 V and less than 5 V.

Temporarily disconnect the Buffer Amplifier output from the VCO input. Adjust the nominal frequency of the VCO to approximately 102.083 kHz. Then remake the connection between Buffer Amplifier and VCO so that the loop is closed again. Adjust the loop gain until phase lock is observed. If you have any difficulty obtaining phase lock, make slight changes to the VCO nominal frequency (with the loop closed) using the tuning knob on the VCO.

You can recognize phase lock as follows. The Frequency Counter will indicate that the VCO output frequency is a stable 102.083 kHz. The oscilloscope will have a stable display for the VCO output (as well as for the 100-kHz carrier). The stable oscilloscope display is the more reliable indicator of phase lock.

Channel A: 100-kHz carrier
Channel B: VCO output (102.083 kHz)

Repeat the above procedure, but setting the VCO nominal frequency to 97.917 kHz. When phase lock is achieved in this case, the Frequency Counter will indicate that the VCO output frequency is a stable 97.917 kHz. Also, this signal will have a stable display on the oscilloscope.

Channel A: 100-kHz carrier
Channel B: VCO output (97.917 kHz)

With the loop closed, experiment with changing the tuning knob of the VCO. You should find that the loop will lock only at the frequencies 97.917 kHz and 102.083 kHz. You should be able to move easily between these two frequencies by a slight change in the VCO tuning knob.

3 Frequency Synthesis of TTL Clock

Build a frequency synthesizer that generates a 75-kHz TTL clock using the 100-kHz TTL clock as the reference. This is accomplished using a phase-locked loop and two frequency dividers:

$$R = 4 \text{ and } N = 3$$

where the $\div 4$ device precedes the loop and the $\div 3$ device is inside the loop. Both frequency dividers are available on the Digital Utilities module.

The switch on the VCO module's PCB should be set to "VCO", and the toggle switch on the front panel should be set to "HI". The nominal frequency of the VCO should be adjusted to approximately 75 kHz. The VCO sensitivity should be adjusted to approximately -1 kHz/V.

When using a phase-locked loop to track a TTL clock, there are two important changes from an analog phase-locked loop. First, the multiplier must be set to "AC" using the toggle switch. This is important because TTL clocks have a DC component (of 2.5 V), and these DC

components must not appear on the multiplier output. Second, the TTL output of the VCO must be used (rather than the analog sinusoidal output).

In building the phase-locked loop, use a Tuneable LPF with its bandwidth adjusted to 10 kHz. Use a Buffer Amplifier between the filter and the VCO input. The negative gain of this amplifier, combined with the negative sensitivity of the VCO, mean that a positive signal at the filter output will cause an increase in the VCO frequency.

Place a copy of the 100-kHz TTL clock on Channel A. Place a copy of the VCO TTL output on Channel B. Use the 25-kHz TTL output of the ÷ 4 device as the external trigger source. Set the trigger level to a value greater than 0 V but less than 5 V.

Adjust the loop gain (by adjusting the gain of the Buffer Amplifier and possibly also the gain of the Tuneable LPF) until phase lock is achieved. If you have any difficulty obtaining phase lock using only adjustments in the loop gain, make slight changes to the VCO nominal frequency (with the loop closed) using the tuning knob on the VCO.

You can recognize phase lock as follows. The Frequency Counter will indicate that the VCO TTL output is a stable 75 kHz. The VCO TTL output will have a stable display on the oscilloscope (with the 25-kHz TTL output of the ÷ 4 device as the trigger source).

Channel A: 100-kHz TTL clock
Channel B: VCO TTL output (75 kHz)

Measure the period of the TTL clock on Channel B. This should equal 13.33 μs, the reciprocal of 75 kHz.

Build a frequency synthesizer that generates, from a 100-kHz reference clock, a TTL clock having a frequency of $(4/3) \times 100$ kHz. This is a frequency of approximately 133.33 kHz. This is accomplished using a phase-locked loop and two frequency dividers:

$$R = 3 \text{ and } N = 4$$

where the ÷ 3 device precedes the loop and the ÷ 4 device is inside the loop. Both frequency dividers are available on the Digital Utilities module.

It is essential that the multiplier in the phase-locked loop be set to "AC" and that the TTL output of the VCO be used.

The nominal frequency of the VCO should be adjusted to approximately 133.33 kHz (that is, 4/3 times 100 kHz). The VCO sensitivity should be adjusted to approximately -1 kHz/V.

The Tuneable LPF should have its bandwidth set to approximately 10 kHz, and a Buffer Amplifier should be placed between the filter and the VCO input.

Place a copy of the 100-kHz TTL clock on Channel A. Place a copy of the VCO TTL output on Channel B. Use the TTL output of the ÷ 3 device as the external trigger source. (The frequency of the external trigger source will therefore be 100/3 kHz.) Set the trigger level to a value greater than 0 V but less than 5 V.

Adjust the loop gain until phase lock is achieved. If you have any difficulty obtaining phase lock using only adjustments in the loop gain, make slight changes to the VCO nominal frequency (with the loop closed) using the tuning knob on the VCO.

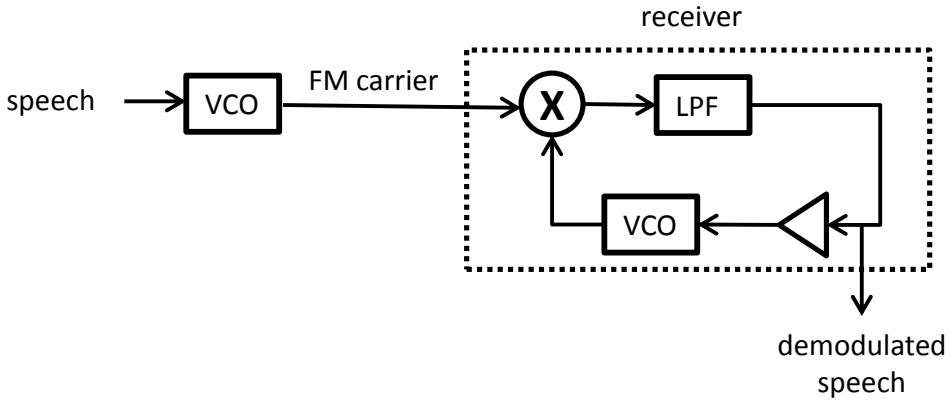
You can recognize phase lock as follows. The Frequency Counter will indicate that the VCO TTL output is a stable 133.33 kHz. The VCO TTL output will have a stable display on the oscilloscope (with the TTL output of the ÷ 3 device as the trigger source).

Channel A: 100-kHz TTL clock
Channel B: VCO TTL output (133.33 kHz)

Measure the period of the TTL clock on Channel B. This should equal 7.5 μs, the reciprocal of 133.33 kHz.

4 FM Demodulation with Phase-Locked Loop

You will create a frequency-modulated carrier, with a speech signal as the message, and then you will demodulate the carrier using a phase-locked loop.



You will use two VCOs. For both of these VCOs, the mode should be set to "VCO" (on the PCB) and the toggle switch on the front panel should be set to "HI". Adjust the nominal frequency of each VCO to approximately 100 kHz. The sensitivity of each VCO should be adjusted to −1 kHz/V.

Place a speech signal on the input of one VCO. The output of this VCO is the frequency-modulated carrier. Observe this FM signal on the oscilloscope. The fluctuating frequency should be apparent.

Build a phase-locked loop using the second VCO, a multiplier, a Tuneable LPF set for a bandwidth of 10 kHz, and a Buffer Amplifier. The negative gain of the Buffer Amplifier will cancel the negative VCO sensitivity, so that a positive signal at the output of the loop filter will cause the VCO output to have a larger frequency than its nominal value.

Place the FM carrier on the input of the phase-locked loop. Place a copy of the FM carrier (the input to the phase-locked loop) on Channel A. Place a copy of the output of the phase-locked loop's VCO on Channel B. Listen to the output of the loop filter, using the headphones.

Adjust the loop gain until phase-lock is achieved. There are two indicators of phase lock. First, the speech signal at the output of the loop filter should become discernible in the headphones (assuming the gain of the Headphone Amplifier is adequate). Second, the phase of the loop VCO output should lead the phase of the FM carrier by approximately 90°. If you have any difficulty obtaining phase lock using only adjustments in the loop gain, make slight changes to the VCO nominal frequency (with the loop closed) using the tuning knob on the VCO.

Because of the frequency modulation, neither of these signals will have a stable display on the oscilloscope. However, if you use the FM carrier as the trigger source with triggering on positive-going zero crossings, the exact center of the display will always contain a positive-going zero crossing of the FM carrier and the phase of the loop's VCO output should be approximately 90° at this point in the display (when the loop is in phase lock). There will be jitter in the phase, due to the correcting (and temporarily over-correcting) action of the feedback circuit, but the average phase of the loop's VCO output should be approximately correct (90° in advance of the FM carrier).

Channel A: FM carrier (input to phase-locked loop)
Channel B: VCO output

Observe the spectra of these two signals. When the loop is in phase lock, these two spectra should be similar. It will be helpful to set the two spectral plots apart, one on top of the other. This can be done like so:

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In the upper spectral plot, only the Channel A signal (the FM carrier) should be displayed. In the lower spectral plot, only the Channel B signal (VCO output) should be displayed.

Channel A: FM carrier (displayed in upper spectral plot)
Channel B: VCO output (displayed in lower spectral plot)

The basic idea of how this demodulation scheme works can be explained as follows. The VCO inside the phase-locked loop is also a frequency modulator. That is, the error signal in the loop

causes changes in the instantaneous frequency at the output of the loop's VCO. The feedback action of the loop causes the instantaneous frequencies of the two VCOs to match. Since these instantaneous frequencies match, the input signals to these two VCOs must match (at least approximately). Therefore, the loop error signal (at the output of the loop filter) should be an approximation of the original speech message.